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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/589,338	06/07/2000	John G. Rohrbaugh	10003687-1	8717

22878 7590 12/16/2002

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EXAMINER
TORRES, JOSEPH D

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 12/16/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/589,338	ROHRBAUGH ET AL.	
	Examin r	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: '218' in Figure 2. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: The Applicant defines a "test sequence" as a series of test vectors in lines 6-7 on page 3 of the Applicant's specification. Hence, a test sequence is a set consisting of test vectors by that definition. In the Applicant's summary (e.g., see lines 1-2 on page 7 of the Applicant's specification), the applicant cites, "each test sequence of the set of test sequences containing a plurality of bits" which contradicts the definition of test sequence that the Applicant has provided since bits are not test vectors.

Appropriate correction is required to clarify the invention.

3. The abstract of the disclosure is objected to because it cites, "each test sequence of the set of test sequences containing a plurality of bits" which contradicts

the definition of test sequence that the Applicant has provided in lines 6-7 on page 3 of the Applicant's specification. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-20 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 1 cites, "each test sequence of the set of test sequences containing a plurality of bits" which contradicts the definition of test sequence that the Applicant has provided since a "test sequence" is defined by the Applicant in lines 6-7 on page 3 of the Applicant's specification to be a series of test vectors and bits are not test vectors.

Claim 15 cites similar language as in claim 5.

Claims 2-4 and 16-20 depend from respective claims 1 and 15, hence inherit the deficiencies of claims 1 and 15, respectively.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-20 rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the relationship between a "test sequence" and a "plurality of bits" in the following phrase cited from claim 1, "each test sequence of the set of test sequences containing a plurality of bits". Note: The Applicant defines a "test sequence" as a series of test vectors in lines 6-7 on page 3 of the Applicant's specification.

Claim 15 cites similar language as in claim 5.

Claims 2-4 and 16-20 depend from respective claims 1 and 15, hence inherit the deficiencies of claims 1 and 15, respectively.

6. The Examiner would like to point out that claims 1-20 are replete with 35 U.S.C. 112 and it is not clear what the phrase "test sequence" refers to whether the Applicant intends "test vector " in place of test sequence, whether the Applicant intends "test vectors" in place of "bits" or whether the applicant has inadvertently left out key essential elements relating a plurality of bits to a "test sequence" as defined by the Applicant in lines 6-7 on page 3 of the Applicant's specification. The Applicant needs to correct all 35 U.S.C. 112 issues in claims 1-20 and, at this point in time, the Examiner is unable to examine the claims on merits to determine patentability.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hosokawa, Toshinori et al. (US 6253343 B1) teaches design for testability and test sequence generation for integrated circuits. Hosokawa, Toshinori (US 6449743 B1) teaches test sequences for use in fault testing for an integrated circuit. Rajski, Janusz et al. (US 6327687 B1) teaches generation and application of test data in the form of patterns, or vectors, to scan chains within a circuit-under-test. Krishnamoorthy, Suresh (US 6237117 B1) teaches a method for testing sequential circuit designs in which an exhaustive sequence of test vectors is applied to the input nodes of edge-sensitive components of a simulated sequential circuit. Rohrbaugh, John G. et al. (US 6067651 A) teaches an improved test pattern generator for compacting test sequences in an automatic test pattern generator. Touba, Nur A. et al. (US 6061818 A) teaches methods for altering bit sequences to improve fault detection in electronic circuits. Chakradhar, Srimat T. et al. (US 5726996 A) teaches automatic testing of integrated circuits and more particularly to a process for developing test sets involving fewer test vectors to increase the rate of testing. Bershteyn, Mikhail (US 5485471 A) teaches partitioning of tailored test vectors into subsets and filling of the subsets with similar vectors starting with vectors close to the initially selected vector and continuing to add vectors farther away until an optimal number of vectors are in the subset. Hosokawa, Toshimori (US 5410552 A) teaches a method and apparatus for generating a test sequence to test a fault in a digital circuit. Patel, Janak et al. (US 5377197 A) teaches a method of generating input vectors for testing electronic circuits.

Motohara, Akira et al. (US 5305328 A) teaches a method of generating test sequences for digital circuits. NN72012510, "Identifying Sources of Unknown Levels Generated during Three Value Fault Simulation". January 1972, IBM Technical Disclosure Bulletin, Vo.: 14, Issue No.: 8, Page No.: 2510 – 2512, January 1, 1972.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.

Joseph D. Torres, PhD
Art Unit 2133
December 4, 2002

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
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